

CLAIMS

What is Claimed is:

1. A round robin arbitration system, comprising:

a first round robin arbitration module having a first bit width and for partitioning a plurality of requests into a plurality of blocks of requests, selecting a block having one or more active requests using round robin arbitration, and generating a first index corresponding to said selected block; and

a second round robin arbitration module having a second bit width and for storing each request of said selected block, selecting each active request of said selected block using round robin arbitration, generating a second index corresponding to said selected active request, and generating a first signal for synchronizing operation of said first and second round robin modules, and wherein said round robin arbitration system has a bit width that is a product of said first and second bit widths.

- 2. A round robin arbitration system as recited in Claim 1 wherein said second round robin module includes a first multiplexor which receives said plurality of requests and outputs, controlled by said first index, said requests of said selected block.
- 3. A round robin arbitration system as recited in Claim 1 wherein said second round robin module includes a first flip-flop for storing said requests of said selected block.

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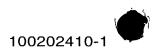
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4. A round robin arbitration system as recited in Claim 1 wherein said second round robin module includes a round robin arbiter which receives said requests of said selected block, selects each active request of said selected block, generates said second index, and generates said first signal.



5. A round robin arbitration system as recited in Claim 1 wherein a second signal is generated based on information from said first and second round robin modules, said second signal indicating whether said first index and said second index are valid.

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6. A round robin arbitration system as recited in Claim 1 wherein said first round robin module includes a reduction-OR circuit for partitioning said requests into a plurality of blocks and for performing an OR operation on each block of requests.

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7. A round robin arbitration system as recited in Claim 6 wherein said first round robin module includes a round robin arbiter which receives output from said reduction-OR circuit, selects said block having one or more active requests, and generates said first index.

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8. A round robin arbitration system as recited in Claim 1 wherein said first bit width is 16 bits, wherein said second bit width is 16 bits, and wherein said bit width is 256 bits.

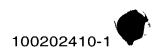
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9. A round robin arbitration system, comprising:

a first round robin arbiter having a first bit width and for selecting a block having one or more active requests using round robin arbitration, and generating a first index corresponding to said selected block; and

a second round robin arbiter having a second bit width and for selecting each active request of said selected block using round robin arbitration, generating a second index corresponding to said selected active request, and generating a first signal for synchronizing operation of said first and second round robin arbiters, wherein said round robin arbitration system has a bit width that is a product of said first and second bit widths.

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10. A round robin arbitration system as recited in Claim 9 further including:

a first multiplexor which receives a plurality of requests and outputs, controlled by said first index, said requests of said selected block; and

a second multiplexor which receives said output of said first multiplexor and has an output, controlled by said first signal, coupled to said second round robin arbiter.

11. A round robin arbitration system as recited in Claim 10 further10 including:

a first flip-flop for storing said requests of said selected block and having an output coupled to said second multiplexor;

a third multiplexor which receives said output of said first multiplexor and said output of said first flip-flop and which has an output, controlled by said first signal, coupled to said first flip-flop; and

a fourth multiplexor which receives a particular value and said second index and has an output, controlled by said first signal, which is coupled said second round robin arbiter.

- 12. A round robin arbitration system as recited in Claim 9 wherein a second signal is generated based on information generated by said first and second round robin arbiters, said second signal indicating whether said first index and said second index are valid.
- 25 13. A round robin arbitration system as recited in Claim 9 further including

a reduction-OR circuit for partitioning a plurality of requests into a plurality of blocks and for performing an OR operation on each block of requests, wherein said reduction-OR circuit has an output coupled to said first round robin arbiter.



- 14. A round robin arbitration system as recited in Claim 13 wherein said first index is coupled to a first multiplexor controlled by a OR circuit which receives said first signal, wherein said first multiplexor is coupled to a first flip-flop, and wherein said first flip-flip is coupled to a second multiplexor controlled by said first signal and is coupled to said first round robin arbiter.
- 15. A round robin arbitration system as recited in Claim 9 wherein said first bit width is 16 bits, wherein said second bit width is 16 bits, and wherein said bit width is 256 bits.

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- 16. A method of arbitrating among a plurality of requests, comprising:
- partitioning said plurality of requests into a plurality of blocks of a) requests;

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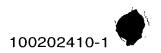
- b) selecting a particular block having one or more active requests using a first round robin arbiter;
 - c) storing each request of said particular block;
- d) selecting each active request of said particular block using a second round robin arbiter; and

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- synchronizing said selecting said particular block and said e) selecting each active request of said particular block.
- 17. A method as recited in Claim 16 wherein said step b) includes generating a first index corresponding to said particular block.

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- 18. A method as recited in Claim 16 wherein said step d) includes generating a second index corresponding to said selected active request.
- 19. A method as recited in Claim 16 wherein said step e) includes 30 generating a first signal for synchronizing operation of said first and second round robin arbiters.



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A method as recited in Claim 16 wherein said plurality of

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requests includes 256 requests, wherein said first round robin arbiter has a 16 bit width, and wherein said second round robin arbiter has a 16 bit width.